WHAT IS CLAIMED IS:

1. A semiconductor storage device comprising:

a memory cell array which data is written into and read from every page; and

control circuit which is connected to said memory cell array and which rewrites at least part of data in data of one page read from an arbitrary page in said memory cell array and which writes the rewritten data into another page in said memory cell array.

2. The semiconductor storage device according to claim 1, wherein said control circuit includes a sense/latch circuit that senses and latches said data of one page read from the arbitrary page in said memory cell array.

3. The semiconductor storage device according to claim 2, wherein said sense/latch circuit includes a plurality of latch circuits.

4. The semiconductor storage device according to claim 3, wherein said plurality of latch circuits are specified according to their addresses, and rewriting of the data is performed by the specified latch circuit.

5. The semiconductor storage device according to claim 4, wherein said control circuit includes a latch specifying circuit which specifies said plurality of latch circuits by the address.

6. The semiconductor storage device according to

claim 5, wherein said latch specifying circuit is a column decoder circuit.

7. The semiconductor storage device according to claim 1, wherein said control circuit includes a page specifying circuit which specifies the page in said memory cell array.

8. The semiconductor storage device according to claim 6, wherein said page specifying circuit is a row decoder circuit.

9. The semiconductor storage device according to claim 2, wherein said control circuit includes a data I/O circuit connected to said sense/latch circuit which outputs data of one page latched by the sense/latch circuit and which gives supplied data to be written to the sense/latch circuit.

10. The semiconductor storage device according to claim 1, wherein said memory cell array comprises a plurality of non-volatile transistors, said plurality of non-volatile transistors are serially connected to form a NAND cells.

11. A semiconductor storage device comprising:

a memory cell array constituted of a plurality of word lines, a plurality of bit lines, and a plurality of memory cells which is connected to said plurality of word lines and said plurality of bit lines, writing and reading of data are performed every page which is constituted of said plurality of memory cells commonly

connected to one word line;

a row decoder which is connected to said plurality of word lines and which selects an arbitrary word line from said plurality of word lines to select an arbitrary page in said memory cell array; and

a sense/latch circuit which is connected to said plurality of word lines and which senses data of one page read from said memory cell array and which latches the sensed data when reading data from said memory cell array and which supplies said memory cell array with the latched data of one page and which rewrites arbitrary data from the latched data of one page when writing data in said memory cell array.

12. The semiconductor storage device according to claim 11, wherein said sense/latch circuit includes a plurality of latch circuits.

13. The semiconductor storage device according to claim 12, further comprising a latch specifying circuit which specifies said plurality of latch circuits by the address.

14. The semiconductor storage device according to claim 13, wherein said latch specifying circuit is a column decoder circuit.

15. The semiconductor storage device according to claim 11, wherein said plurality of memory cells is each constituted of non-volatile transistor, and a plurality of non-volatile transistors are connected in

series to form a NAND cell.

16. The semiconductor storage device according to claim 11, further comprising a data I/O circuit which is connected to said sense/latch circuit and which outputs data of one page latched by said sense/latch circuit and which gives supplied data to be written to said sense/latch circuit.

17. An operation method of a semiconductor storage device, comprising:

reading data in parallel from a plurality of memory cells in a certain memory area of a non-volatile semiconductor storage device that has a plurality of memory areas each including a plurality of memory cells;

latching said read data by a plurality of latch circuits, and rewriting at least part of said data latched by said plurality of latch circuits; and

writing said data at least part of which is rewritten into said plurality of memory cells of said memory area which is different from said memory area from which said data is read.